DIGIPREDICT

Quadro-channel organ-on-chip for modeling and studying the blood-brain barrier

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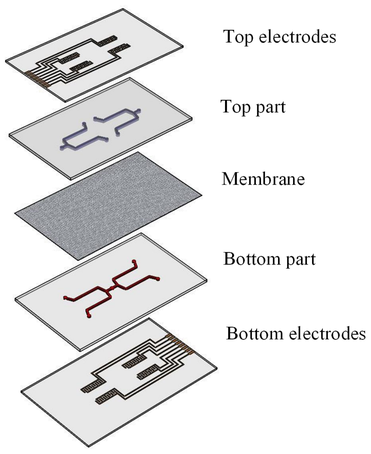
1. Introduction

Different organs have already been successfully emulated and studied in various chip designs [1]. However, most of them have **low-throughput** workflows and lack **real–time monitoring** and **sensing.**

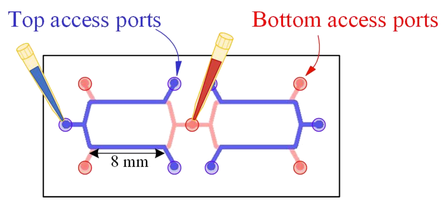
We present a design of an organ–on–chip (OoC) device emulating the blood-brain barrier (BBB), which allows studying this organ in fourfold with the potential to integrate electrodes for real-time monitoring of the barrier formation using transendothelial electrical resistance (TEER) measurement.

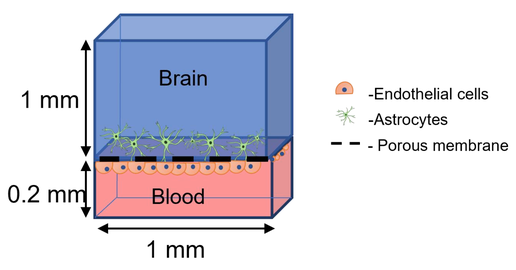
2. Chip design



The designed OoC is a 5-layers sandwich-like polydimethylsiloxane (PDMS) device with 4 channels in the top and bottom parts separated by a 2 µm thick PDMS membrane.

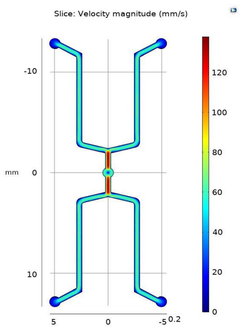
The **top** 4 channels are designed for abluminal culture. The **bottom** part representing the luminal compartment has 4 channels branching from the one central inlet and has separate outlets.





3. Simulations

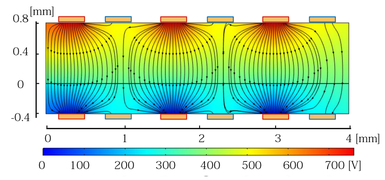
Laminar flow COMSOL study showed that the design guarantees an equal distribution of cells when seeding through the common inlet.



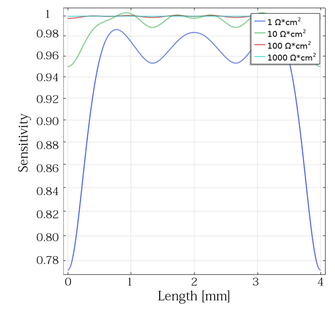
For the correct TEER measurement, electrode placement is crucial [2].

The sensitivity of the electrodes was tested using **COMSOL ec, stationary** study.

A



B



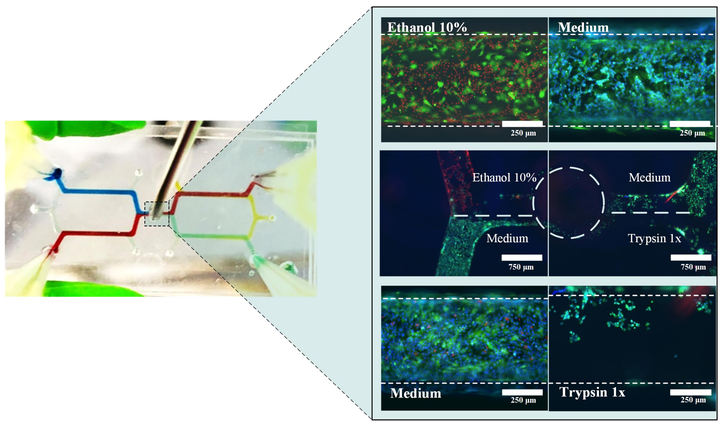
COMSOL simulation of the electric field and current density distribution in the channels with a 4-point measurement setup

Sensitivity distribution along the channel length with the sensitive areas close to 1, meaning a homogeneous measurement of the cell layer.

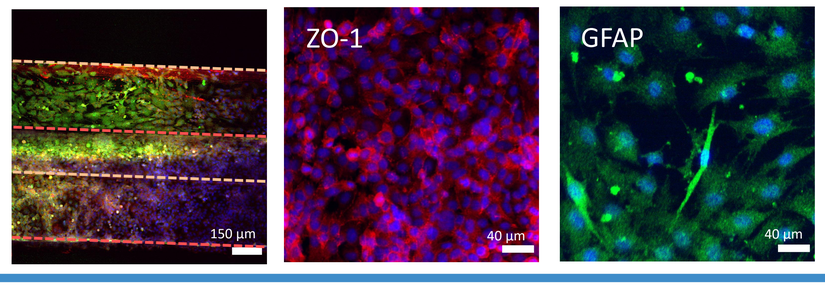
4. Results

An example of the possibility to create four different conditions in the bottom channels.

Live-Dead

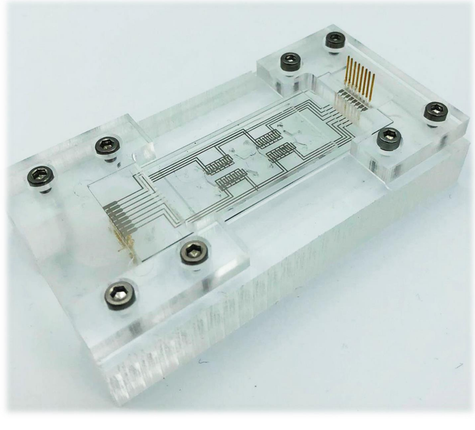


The BBB was modeled by seeding hCMEC/D3 and human astrocytes in the bottom and top compartments respectively.



5. Conclusion and outlooks

- We designed a new chip that consists of **4** channels that require only **1** pump to address all of them.
- We modeled a BBB in **quadruple** and showed how the channels can be individually addressed.
- The TEER measurement can be performed by integrating the electrode array in the top and bottom of the chip.



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[1] J.E. Sosa-Hernández, et.al., Micromachines 2018, Vol. 9, Page 536 **2018**, 9, 536.
[2] J. Yeste, X. Illa, et.al., J. Phys. D. Appl. Phys. **2016**, 49.

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